REMARKS

This responds to the Office Action mailed on August 23, 2007. Reconsideration is respectfully requested.

Claims 1, 2, 6, 9, 22, 24, 47, 68, 69 and 70 are amended, claims none are canceled, and claims none are added; as a result, claims 1 – 62 and 64 - 71 remain pending in this application.

§112 Rejection of the Claims

Claims 68 and 69 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Claims 68 and 69 have been amended to depend from claim 47. Accordingly, Applicant submits that the rejection of claims 68 and 69 under 35 U.S.C. § 112 has been overcome.

§102 Rejection of the Claims

Claims 1-18, 20-62, and 64-71 were rejected under 35 U.S.C. § 102(e) for anticipation by Borland et al. (U.S. 6,724,772).

Applicant's claim 1, for example, is directed to a digital processing integrated circuit to process media data. Claim 1, as amended, recites that the integrated circuit comprises a data path arranged within the integrated circuit in a ring configuration, a plurality of processing modules positioned within the data path to process the media data, and a digital interface to communication with a device external to the integrated circuit. Claim 1 further recites that the data path comprises a plurality of separate portions to communicate data between adjacent of the processing modules. Claim 1 further recites that the separate portions of the data path couple the adjacent processing modules in series to communicate the media data between the adjacent processing modules. Claim 1 further recites that media data is clocked between the adjacent processing modules around the separate portions of the data path to provide communications from a source processing module to a target processing module. Claim 1 further recites that when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules. Claims 22, 24 and 47 have similar recitations.

Because each separate portion of the data path couples two adjacent processing modules in series, data on the data path can only be communicated directly between adjacent processing modules, and data on the data path cannot be communicated directly between non-adjacent processing modules because there is no direct communication path coupling non-adjacent processing modules. Media data can be clocked directly between a source processing module and a target processing module when the source and target processing modules are adjacent, however, when the source and target processing modules are non-adjacent, the media data is clocked through one or more intervening processing modules.

Support for the amendment to claims 1, 22, 24 and 47 can be found throughout Applicant's specification. For example, Applicant's FIG. 1 shows that processing modules are positioned within data path 22, and that data path 22 comprises separate portions between the processing modules. The separate portions of data path between the processing modules is further illustrated in Applicant's FIG. 5 which shows the input side and the output side of the separate portions of data path 22 and that any data on data path 22 is clocked through a processing module.

In Borland, there are no separate portions of a data path, and the processing modules are not *positioned within* the data path, as recited in Applicant's claims 1, 22, 24 and 47. Borland teaches a single bus 330 in which all modules 210A-210H can access. In Borland, there are no separate portions of the bus and data on the bus is accessible by all modules (see Borland FIG. 3). Note that Borland's modules 210A-210H are not positioned within the data path of bus 330.

According to the Examiner, Borland's data bus interconnects the plurality of processing modules in series (see the Office Action dated 8/23/08 page 18 line 1). Applicant disagrees with this interpretation of Borland and submits that because any module 210A-210H can access the data on data bus 330 at any time, there is no restriction limiting the order in which the processing modules can access the data. Furthermore, in Borland, there is no restriction on what data any module can access. For example, data on bus 330 from module 210A does not have to be processed or go through module 210B before it can be processed by module 210C. Module 210C can directly access data provided by module 210A on bus 330 (see Borland FIG. 3). In Borland, non-adjacent modules (i.e., modules 210A and 210C) can communicate directly without having to pass the data through an intervening module (i.e., module 210B). Applicant's claim 1, on the

other hand, recites that when a source and a target processing module are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules. This is not the case in Borland since all modules access the same bus.

Accordingly, claims 1, 22, 24, and 47 are believed to be allowable over Borland. Claims 2 – 21 are believed to be allowable at least because of their dependency on claim 1. The other dependent claims are believed to be allowable at least because of their dependency on either claim 22, 24, or 47.

Claim 2, as amended, further distinguishes over Borland and emphasizes the configuration of Applicant's data path by reciting that media data is communicated around the ring configuration in a single direction between the adjacent processing modules.

Claim 9, as amended, further distinguishes over Borland and emphasizes the operation of the separate portions of the data path. Claim 9 recites that media data is selectively extracted for processing from a first of the separate portions of the data path, and that the media data is provided in at least one time-slot of the first portion of the data path allocated to the processing module. Claim 9 further recites that processed media data is selectively inserted into its allocated time-slot on a second of the separate portions for receipt by a next processing module. Claim 9 further recites that media data that it receives and that is associated with other processing modules is passed unchanged along the second of the separate portions for receipt by the next processing module. In Borland, a processing module would never need to pass along data unchanged because all modules 210A – 210H access the same data path (i.e., bus 330) and can simply refrain from accessing data on the bus (see Borland FIG. 3).

Claim 70, as amended, further distinguishes over Borland and emphasizes single direction communication around the ring by reciting that that each processing module includes an input to receive data sent by a first adjacent processing module over a first of the separate portions, and an output to send data to a second adjacent processing module over a second of the separate portions to allow serial interconnection of the processing modules in the ring configuration.

One purpose of Borland's invention is to address the different capabilities of various modules in a large computer system by providing a single bus with variable bandwidth capability (see Borland, column 1, lines 29 – 49). In Borland's system, as with most computer systems, all

modules must be able to access a common bus, which is emphasized in Borland column 1 lines 50 – 61). Applicant submits that the use of a single common bus ***teaches away*** from Applicant's claims 1, 22, 24, and 47, for example, which recite the clocking of media data between adjacent processing modules over separate portions of a data path. With this configuration, media data can be added or retrieved from the data path by a processing module as data is clocked between adjacent processing modules. Applicant's claims 14 and 23, for example, emphasize this by reciting that while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path. Thus, not only does Borland no anticipate Applicant's claims 1, 22, 24, and 47, Borland cannot be combined with one or more other references.

§103 Rejection of the Claims

Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Borland et al. According to the Examiner, Borland does not disclose a transport bus to communicate data between an external memory that is separate from the integrated circuit and at least one of the processing modules. In view of the discussion above, Applicant submits that claim 19 is allowable at least because of its dependency on claim 1 and that the rejection of claim 19 under 35 U.S.C. § 103(a) has been overcome.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 480-659-3314 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17th, day of October 2007.

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